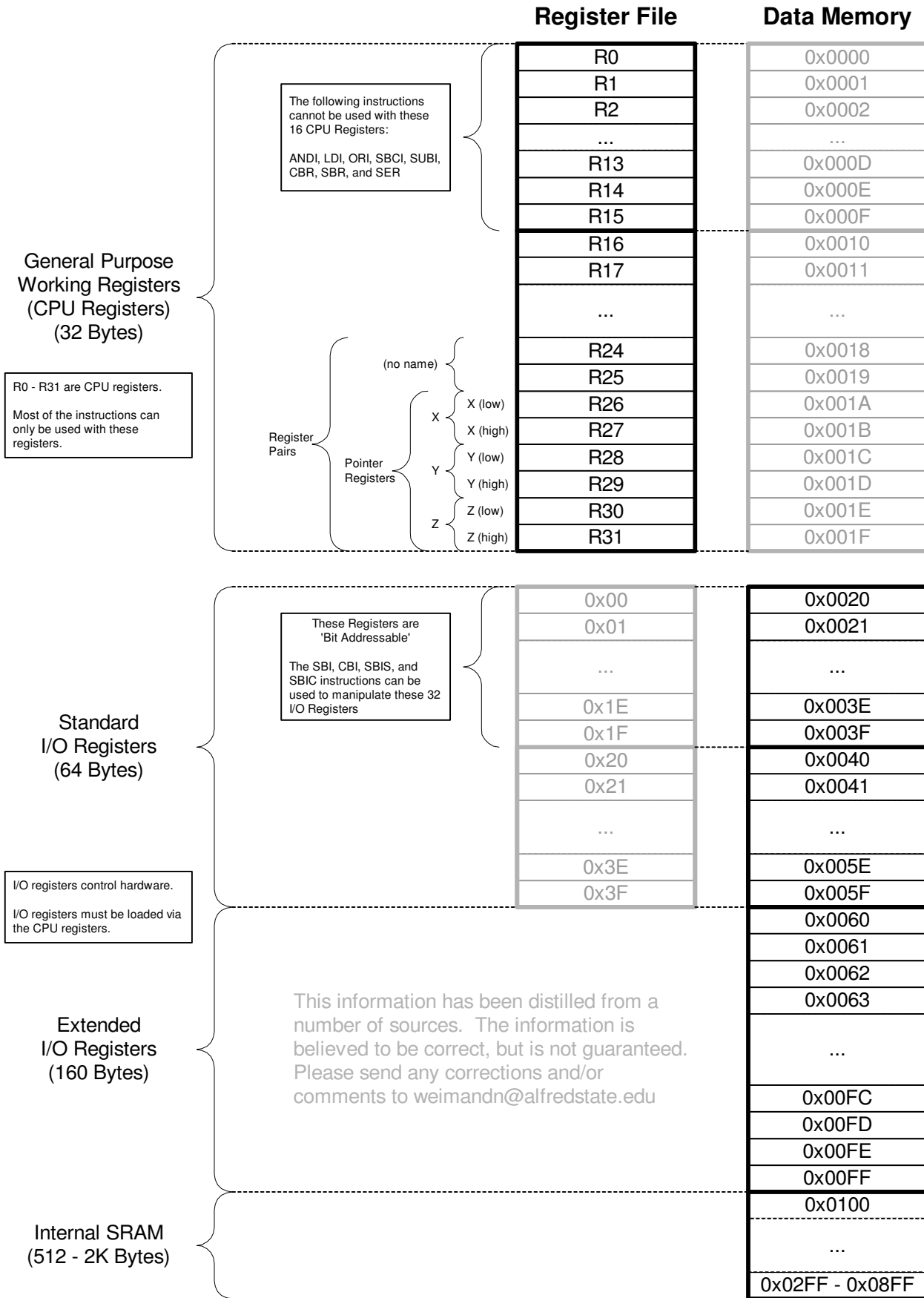


ATmega SRAM Data Memory

ATmega48/88/168/328 etc.



General Purpose Working Registers (CPU Registers) (32 Bytes)

R0 - R31 are CPU registers.
Most of the instructions can only be used with these registers.

The following instructions cannot be used with these 16 CPU Registers:
ANDI, LDI, ORI, SBCL, SUBI, CBR, SBR, and SER

Register Pairs
 (no name) {
 X { X (low)
 X (high)
 Y { Y (low)
 Y (high)
 Z { Z (low)
 Z (high)

Standard I/O Registers (64 Bytes)

I/O registers control hardware.
I/O registers must be loaded via the CPU registers.

These Registers are 'Bit Addressable'
The SBI, CBI, SBIS, and SBIC instructions can be used to manipulate these 32 I/O Registers

Extended I/O Registers (160 Bytes)

This information has been distilled from a number of sources. The information is believed to be correct, but is not guaranteed. Please send any corrections and/or comments to weimandn@alfredstate.edu

Internal SRAM (512 - 2K Bytes)